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# Electronic properties of nonpolar cubic GaN MOS structures

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The electric characteristics of non-polar cubic gallium nitride (GaN) metal-oxide-semiconductor (MOS) capacitors were measured by capacitance (C-V) and conductance ($G_p/\omega$–F) techniques. From the hysteresis in the C-V curve and the peak height of the $G_p/\omega$ - frequency curves a maximum interface state density $D_{it}$ of ~$2x10^{13}$ $cm^{-2}eV^{-1}$ is estimated. An interface trap band existing about 0.3 eV below the conduction band is measured in non-polar cubic gallium nitride (GaN).



**1 Introduction** State of the art AlGaN/GaN heterojunction field effect transistors (HFETs) are fabricated on c-plane faces of the stabile wurtzite crystal structure with inherent spontaneous and piezoelectric polarization fields which produce extraordinarily high sheet carrier concentration at the hetero-interface. Therefore, these devices exhibit *normally on* operation due to the high-density two-dimensional electron gas under the gate. For power and consumer applications, however, normally-off operation is required to simplify the design of driving circuits and for the safety of the products. Several techniques for the normally-off operation of the AlGaN/GaN HFET have been reported, such as using a thin AlGaN barrier layer, a recess gate structure, a fluoride-based plasma treatment and a non-polar GaN channel [1-5]. Recently, nearly *normally off* operation has been realized on a non-polar *a*-plane AlGaN/GaN HFET in which the threshold voltage is only - 0.5V and where polarisation effects are avoided [6]. However, a direct way to fabricate HFETs without undesirable parasitic polarization effects is the growth of *cubic* group III-nitrides. [7].

The high gate leakage current of GaN-based HFETs pushes their development into the use of metal/oxide stacks instead of a Schottky gate leading to the metal-oxide-semiconductor transistors (MOS-HFET) [8, 9]. To achieve a sufficient high quality of the interface between the oxide and nitride epilayer is one critical issue of such devices. Thus it is important to accurately characterize this interface in order to better understand and model devices with such interfaces.

In this paper we report on capacity vs. voltage (C-V) and conductance vs. frequency ($G_p/\omega$–F) characteristics of metal/$SiO_2$/cubic GaN MOS structure at room temperature and measure the interface state density $D_{it}$.

**2 Experimental** 600 nm thick phase-pure cubic GaN epilayers were grown on highly conductive free-standing 3C-SiC substrates in a Riber 32 system by plasma-assisted molecular beam epitaxy (MBE). We exploited reflection high energy electron diffraction (RHEED) for in-situ growth control. In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness a coverage of 1 monolayer Ga was established during growth [7]. The full width at half maximum (FWHM) of the cubic GaN (002) rocking curve was about 20 arcmin and the background carrier concentration was about $6x10^{16}cm^{-3}$ as measured by C-V measurements. A 65 nm thick $SiO_2$ layer was deposited by plasma enhanced chemical vapour deposition (PECVD) at 300 °C. On top of the $SiO_2$ oxide Ti/Al/Ni/Au (15nm/50nm/15nm/50nm) gate contacts with a diameter of 100µm were thermally evaporated. As second contact a large area In back side contact to the 3C-SiC substrate was used.

The MOS capacitors were characterized by means of C-V and G/ω–F measurements using an Agilent E4980A LCR meter. The dc bias was varied from deep depletion to

accumulation and then back to deep depletion. An ac-amplitude of 50 mV was used and the measurements were performed under light-tight and electrically shielded environment. Interface trap density values $D_{it}$ have been extracted by the conductance method [10].

**3 Results and discussion** Typical C-V curves of the cubic GaN MOS structure measured at frequencies of 1 MHz, 100 kHz and 10 kHz are shown in Fig. 1. The measured capacity was normalized to the oxide capacity $C_{ox}$. The solid black curve represents the ideal MOS capacitor without interface and oxide charges [11, 12]. The flat band voltage $V_{FB}$ = 0.2 V results from the difference in work function of the metal (Ti 4.3 eV) and electron affinity of cubic GaN (4.1 eV). For the simulation dielectric constants for $SiO_2$ ($\varepsilon_r$ = 3.9) and GaN ($\varepsilon_r$ = 5.35) were used. A net donor density of $N_D = 6\text{x}10^{16}$ cm$^{-3}$ for GaN was obtained by fitting the $1/C^2$ versus V data and the intrinsic carrier concentration in GaN was assumed to be $1\text{x}10^{-6}$ cm$^{-3}$, respectively. The measured accumulation capacitance was used to determine the equivalent oxide thickness (EOT) of 65 nm. The simulated curve is in excellent agreement with the measured C-V curve for all measuring frequencies when the dc bias was swept from deep depletion to accumulation. However, for the bias sweep back to depletion the C-V curve shows a positive shift of about 4 V from the ideal curve. A hysteresis in the C-V curves of a $SiO_2$/GaN MOS capacitor indicates the existence of a small amount of interface traps. For negative bias voltages no inversion capacitance is observed even at the lowest frequency of 10 kHz and the capacitance continues to drop below the calculated value $C_{min}$ indicated in Fig. 1. This deep depletion feature is typical for wide-gap semiconductor MOS structures, because the generation rate of the minority carriers (holes) is extremely low at room temperature. The extremely low hole generation rate means that the electron quasi-Fermi level will remain unchanged due to the large time constant. It can then be argued that any change in interface charge must be a result of the capture of electrons.

A more sensitive technique for characterizing insulator-semiconductor interface properties relies on characterizing the interface trap conductance due to its direct measuring of the energy loss during capture and emission of the majority carriers (electrons) between conduction band and interface trap levels under applied AC signal [11, 12]. After series and oxide capacitance correction, the remaining parallel conductance $G_p$ value only includes interface trap information. Figure 2 shows $G_p/\omega$ - frequency curves for different bias voltages between -1 V and 10 V. Within the measured frequency range from 1 kHz to 2 MHz the $G_p/\omega$ curves shows a clear peak for the biases between -1 V and +1 V. The peak shifts to higher frequencies at positive voltages and simultaneously the peak intensity is reduced.

The equivalent parallel conductance $G_p$ divided by $\omega$ which does not contain the depletion capacity $C_D$ and depends only on the interface-trap, is given by [13] where

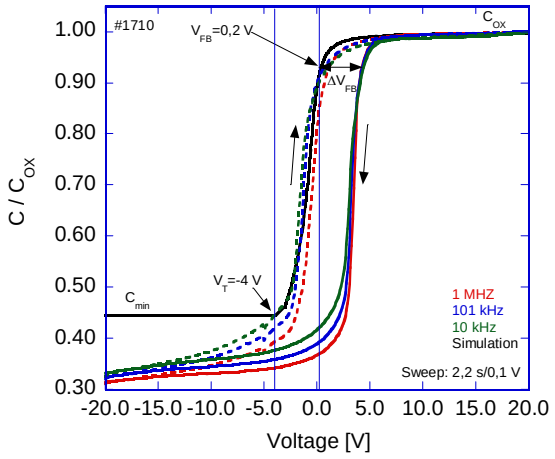


**Figure 1** Hysteresis C-V curves of a cubic GaN MOS structure measured at frequencies of 1 MHz, 100 kHz and 10 kHz. The full black curve shows a simulation of the ideal structure.

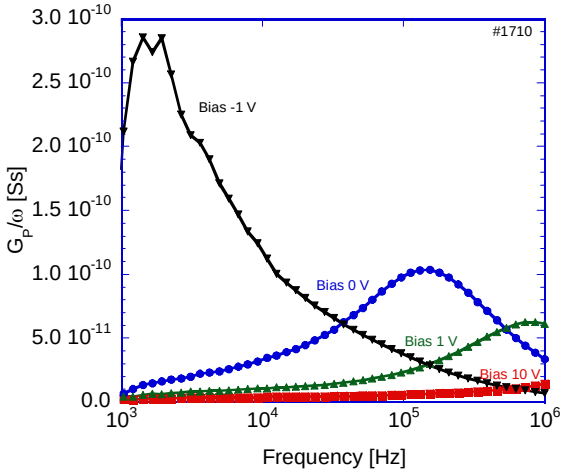


**Figure 2** Conductance $G_p/\omega$ versus frequency curves of a cubic GaN MOS structure at several biases.

$$\frac{G_P}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} = \frac{C_{it}\,\omega\,\tau_{it}}{1 + \omega^2 \tau_{it}^2} \qquad (1)$$

$\omega=2\pi f$ and $\tau_{it}$ is the interface trap lifetime. At a given bias, the plot of $G_p/\omega$ versus $\omega$ goes through a maximum when $\omega\tau_{it}$ = 1, and gives $\tau_{it}$ directly. The value of $G_p/\omega$ at the maximum is $C_{it}/2$, where the $C_{it}$ is the capacity associated to the interface traps. Once $C_{it}$ is known, the interface trap density is obtained by using the relationship

$$D_{it}=C_{it}/q^2\,. \qquad (2)$$

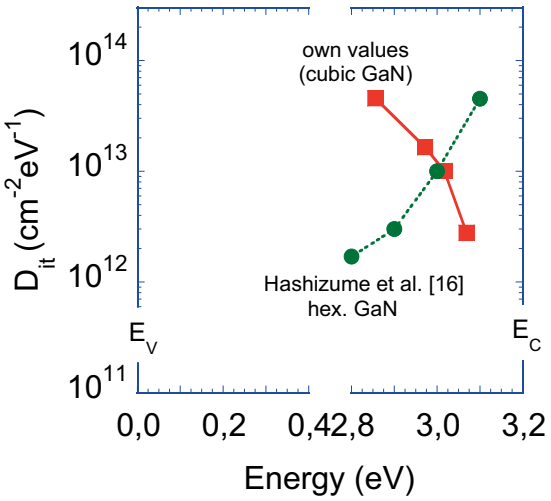


**Figure 3** Interface density $D_{it}$ vs. energy within the band gap of a cubic $SiO_2$/GaN MOS structure. (red squares own data, green full circles data from Ref. [16]).

The interface trap time constant $\tau_{in}$ is given by the Shockley-Read-Hall model [14]

$$\tau_{it}(E) = \frac{1}{\sigma_{0n} v_{th} N_c} \cdot \exp\left(\frac{E_c - E}{k_B T}\right) \qquad (3)$$

where $N_c$, $v_{th}$, $\sigma_{0n}$, $E_c$, $k_B$ and T are the effective density of states in the conduction band, the thermal velocity of electrons, the capture cross section of the trap, the bottom of the conduction band, the Boltzmann constant, and temperature, respectively. In this way the frequency $f_{max}$ at the maximum of $G/\omega$ gives $\tau_{it} = 1/2\pi f_{max}$ and correlates $f_{max}$ to a corresponding trap energy level E below conduction band. Considering the parameter values from Eq. (3) the thermal velocity and density of state are well known and well defined for a specific semiconductor, whereas the trap capture cross section $\sigma$ depends strongly on the nature of the trap. The capture cross section can take values varying from $10^{-12}$ to $10^{-20}$cm$^{-2}$. Since the majority of trapping states has $\sigma$ values of the order of $10^{-15}$cm$^{-2}$ [15] we assume this value to convert the $\tau_{it}$ into trap energies below the conduction band in order to illustrate the effects.

In Fig. 3 the distribution of interface state density $D_{it}$ calculated from the peak maximum of $G_p/\omega$ vs f is plotted for cubic GaN. An increase of $D_{it}$ (E) with energy depth below the band gap of the cubic GaN is observed. This indicates a defect band existing about 0.3 eV below the conduction band. This observation is opposite to that seen in hexagonal c-plane GaN, where a decrease interface states $D_{it}$ is observed [16, 17]. For comparison some values reported in Ref. [16] have also been plotted in Fig. 3. The nature of this different behavior for cubic and hexagonal GaN has to be investigated in future and the PECVD process for our $SiO_2$ deposition has to be optimized to reduce this acceptor like interface traps.

**4 Conclusions** An interface trap band existing about 0.3eV below the conduction band has been observed in non-polar cubic gallium nitride (GaN) metal-oxide-semiconductor (MOS) capacitors by measuring the electrical properties of $SiO_2$/cubic GaN MOS capacitors with capacitance and conductance techniques. A maximum interface state density $D_{it}$ of ~2x10$^{13}$ cm$^{-2}$eV$^{-1}$ is estimated.

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