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Cubic AlGaN/GaN Hetero-field effect transitors with normally on and normally off operation

D.J. As[1], E. Tschumak[1], F. Niebelschütz[2], W. Jatal[2], J. Pezoldt[2], R. Granzner[3], F. Schwierz[3], and K. Lischka[1]
[1)] Universität Paderborn, Department Physik, Warburger Strasse 100, 33098 Paderborn, Germany
[2)] FG Nanotechnologie, Institut für Mikro- und Nanotechnologien, TU Ilmenau, Postfach 100565, 98684 Ilmenau, Germany
[3)] FG Festkörperelektronik, TU Ilmenau, Postfach 100565, 98684 Ilmenau, Germany

ABSTRACT

Non-polar *cubic AlGaN/GaN HFETs* were grown by plasma assisted MBE on 3C-SiC substrates. Both normally-on and normally-off HFETs were fabricated using contact lithography. Our devices have a gate length of 2 µm, a gate width of 25 µm, and source-to-drain spacing of 8 µm. For the source and drain contacts the $Al_{0.36}Ga_{0.64}N$ top layer was removed by reactive ion etching (RIE) with $SiCl_4$ and Ti/Al/Ni/Au ohmic contacts were thermally evaporated. The gate metal was Pd/Ni/Au. At room temperature the DC-characteristics clearly demonstrate enhancement and depletion mode operation with threshold voltages of +0.7 V and –8.0 V, respectively. A transconductance of about 5 mS/mm was measured at a drain source voltage of 10 V for our cubic AlGaN/GaN HFETs, which is comparable to that observed in non-polar a-plane devices. From capacity voltage measurements a 2D carrier concentration of about $7x10^{12}\,cm^{-2}$ is estimated. The influence of source and drain contact resistance, leakage current through the gate contact and parallel conductivity in the underlaying GaN buffer are discussed.

INTRODUCTION

AlGaN/GaN heterojunction field-effect transistors (HFETs) are presently of outstanding interest for electronic devices, in particular, for high-power and high-frequency amplifiers. This is motivated by the potential commercial and defense applications, e.g., in the area of communication systems, radar, base stations, high-temperature electronics and high-power solid-state switching [1, 2]. Currently, state of the art AlGaN/GaN HFETs are fabricated of c-plane surface material of the stabile wurzite crystal structure with inherent spontaneous and piezoelectric polarization fields which produce extraordinary high sheet carrier concentration at the heterointerface. Therefore, usually these devices are of the *normally-on* type. However, for power and consumer applications, *normally-off* operation is required to simplify the design of driving circuits and for the safety of the products. A direct way to fabricate HFETs without undesirable parasitic polarization effects is the use of *cubic* group III-nitrides.

If the cubic group-III nitrides are grown in (001) direction spontaneous and piezoelectric polarization effects can be avoided at the interfaces and surfaces and the density of the two-dimensional electron gas (2-DEG) in cubic $Al_xGa_{1-x}N$/GaN heterostructures is independent on the thickness and Al mole fraction of the $Al_xGa_{1-x}N$ barrier layer and can be controlled by doping with silicon. The combination of these effects may be used to realize cubic AlGaN/GaN HEMTs with both *normally on* and *normally off* operation as it is strongly required for logic devices [3].

In addition, the electronic structure of the cubic GaN (001) surface is different to that of the c-plane in hexagonal GaN and therefore may alters the electronic properties of the Schottky diodes and ohmic contacts [4].

In this work, non-polar *cubic AlGaN/GaN HFETs* were grown by plasma assisted MBE on 3C-SiC substrates. Both normally-on and normally-off HFETs were fabricated using contact lithography and normally on and normally off operation is demonstrated.

EXPERIMENT

For the epitaxy of cubic AlGaN/GaN hetero structures, freestanding Ar^+ implanted 3C-SiC was used. Previous to the Ar^+ implantation, the carrier concentration in the 3C-SiC substrate of $n=2\times10^{18}$ cm^{-3} was measured by Hall effect. A three energy implantation with Ar ions at doses of 6×10^{14} cm^{-2} at 160 keV, 2.4×10^{14} cm^{-2} at 80 keV and 1.2×10^{14} cm^{-2} at 40 keV was used to form a damage layer near the surface. We showed that this damage acts as insulation layer [5]. Reflection high energy electron diffraction (RHEED) was used to monitor the crystalline nature of the sample surface. Streaky RHEED patterns were observed for both the surface of the Ar^+ implanted 3C-SiC and for the surface of a 600 nm thick cubic GaN (c-GaN) grown on this substrate revealing a two dimensional surface condition.

Cubic $Al_xGa_{1-x}N$/GaN hetero structures were grown in a Riber 32 system by plasma-assisted molecular beam epitaxy. Prior to growing process, the substrate was chemically etched by organic solvents and buffered oxide etching (BOE). In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness, coverage of one monolayer Ga was established during growth [6]. The substrate temperature was 720°C and the growth rate was 115 nm/h.

Two different cubic Al_xGaN_{1-x}/GaN heterostructures (Sample A and Sample B) with similar crystalline properties were investigated. The full width at half maximum (FWHM) of the cubic GaN (002) rocking curve was 25 arcmin. In both samples, the cubic $Al_xGa_{1-x}N$ was pseudomorphically strained on the cubic GaN, measured by reciprocal space mapping [7]. The RMS roughness of the surface measured by AFM in a 5×5 μm^2 scan was 5 nm.

RESULTS AND DISCUSSION

HFET with normally-off characteristics

Sample A consists of 600 nm unintentionally doped (UID) cubic GaN followed by 3 nm UID cubic $Al_{0.25}Ga_{0.75}N$ spacer layer, 2 nm cubic $Al_{0.25}Ga_{0.75}N$:Si and 15 nm UID cubic $Al_{0.25}Ga_{0.75}N$. The carrier concentration of the Si doped AlGaN layer is $n=4.5\times10^{18}$ cm^{-3}. A 5 nm thick heavily silicon doped cubic GaN:Si cap with a carrier concentration of $n=6\times10^{19}$ cm^{-3} was grown on top of the sample. For ohmic source and drain contacts, Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated on GaN:Si and annealed at 850°C for 30 s in nitrogen environment. Then, mesa insulation was performed with $SiCl_4$ RIE down to the substrate. For the gate contact, the GaN:Si cap layer was removed using RIE with $SiCl_4$ down to the substrate. The gate was fabricated by evaporation of Pd/Ni/Au (15 nm/15 nm/50 nm) and a subsequent annealing processs at 400°C for 10 min. The device had a gate length of 2 µm, a gate

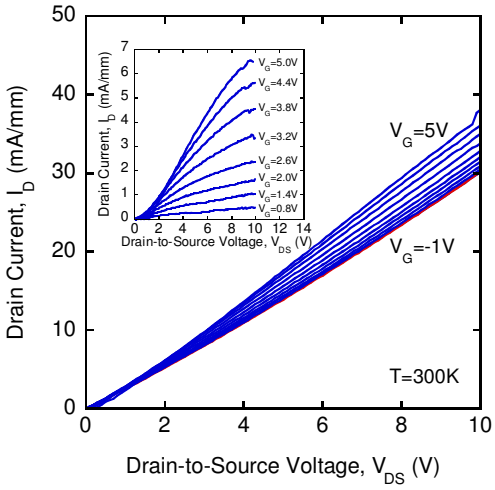

Figure 1. *Drain current I_{DS} vs. drain source voltageV_{DS} of HFET A. The inset shows the same measurement curves corrected for the drain current at V_{GS}=-1 V.*

width of 25 µm and a source-to-drain spacing of 8 µm. 250 nm of SiO_2 was deposited around the device to insulate the contact pads electrically.

The room temperature DC drain current-voltage curves with gate-to-source voltages from -1 V to + 5V of HFET Sample A are displayed in Fig. 1. The threshold voltage of this device is +0.7 V measured at V_{DS} =10 V by extrapolation of the transconductance curve (not shown here). This indicates a normally-off device characteristics, however, the drain-to-source current at V_G = 0 V is relatively large due to the high conductivity of c-GaN buffer layer. The inset shows the measurement data adjusted by the shunt current. A maximum drain-to-source current of 6.5 mA/mm was observed when a gate voltage of +5 V was applied.

In Table I the experimental data of our cubic normally off HFET is compared with hexagonal state of the art nonpolar a-plane HFETs and c-plan HFETs [8]. The transconductance g_m of about 3 mS/mm of our cubic device compares well with that of the non-polar a-plane devices. For our cubic device, however we clearly measured a positive threshold voltage of + 0.7 V, whereas for the a-plan devices only "nearly positive" V_{th} of - 0.5 V are observed. In addition, cubic HFET show no dependence on the orientation of the gate as observed in a-plan HFET (compare columns 3 and 4 in Table I). Compared to c-plane HFET, which only shows *normally on* behavior, the transconductance is nearly a factor of 30 lower. We attribute this fact to the still inferior material quality of cubic or a-plane GaN compared to c-plan GaN and to the fact that the dislocation density, which reduces the carrier mobility and therefore g_m, is at least one order of magnitude higher in the non-polar nitrides.

Table I: Summary of device performance of cubic, a-plane with gate in [1-100] and [0001] direction and c-plane AlGaN/GaN HFETs [8].

	cubic HFET	**a-plane HFET gate in [1-100]**	**a-plane HFET gate in [0001]**	**c-plane HFET**
$I_{DS\ max}$ (mA/mm)	6.5	19.5	13.5	423
$g_{m\ max}$(mS/mm)	3	6.7	3.6	112
V_{th}(V)	+ 0.7	- 0.5	- 0.5	- 4.0
L_G (µm)	2	1	1	1

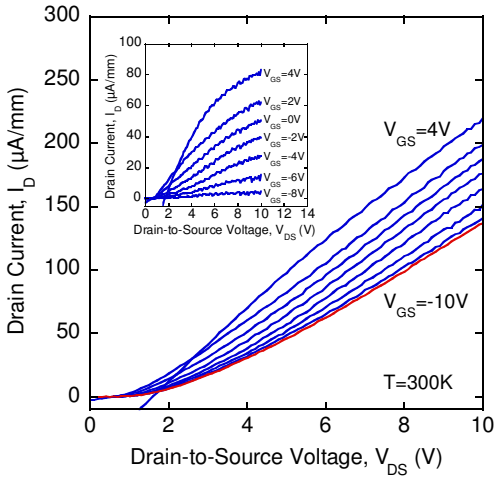

Figure 2. *Static output characteristics of the HFET B. The inset shows the same measurement curves corrected for the drain current at V_{GS}=-10 V.*

HFET with normally-on characteristics

To minimize the shunt current through the cubic GaN buffer layer, carbon doping using CBr_4 [9-11] was tested in Sample B. Sample B consists of a 60 nm UID cubic GaN nucleation layer followed by 580 nm carbon doped cubic GaN:C. For the carbon doping a CBr_4 beam equivalent pressure (BEP) of 1×10^{-6} mbar was used. A 34 nm thick homogeneously doped $Al_{0.36}Ga_{0.64}N$:Si cap with a carrier concentration of $n=1.5\times10^{18}$ cm^{-3} was grown on top of the sample. For the source and drain contacts, 10 nm of the $Al_{0.36}Ga_{0.64}N$ top layer were removed by reactive ion etching (RIE) with $SiCl_4$. After that Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated and annealed at 850°C for 30 s in N_2 environment. Then the Pd/Ni/Au gate contact was fabricated as described for HFET A. The device geometry was the same as for HFET Sample A.

The room temperature output characteristics of HFET Sample B are depicted in Fig. 2. The gate-to-source voltage was varied between -10 V and +4 V. Apart from the shunt current through the 3C-SiC substrate and GaN:C buffer layer (red curve), a clear field effect with normally-on characteristics is measured in this sample. The inset shows the same measurement data adjusted by the shunt current. The measurements of the source and drain contact resistance showed a slight non ohmic behaviour which limited the absolute current through the device. Therefore, the source-to-drain current difference between V_G=-10V and V_G=+4 V was 80 µA/mm only. At high positive gate voltages, an additional gate leakage is observed at low source-to-drain voltages. So, the drain current at +4 V gate voltage is reduced by the gate leakage.

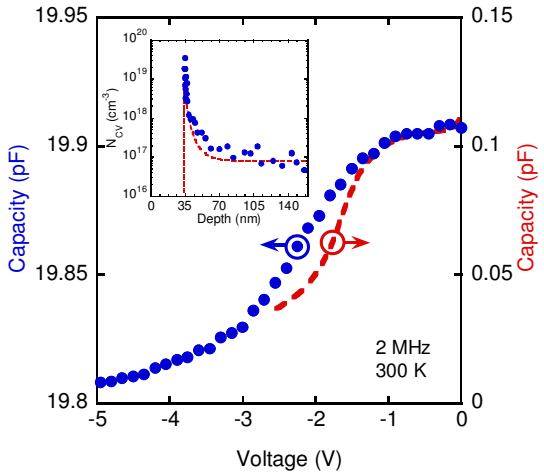

Figure 3. *CV characteristics of HFET B measured on the gate contact at 2 MHz confirming the presence of an electron channel at the AlGaN/GaN interface. The inset shows a carrier density profile N_{CV}. The red dashed lines are CV curves calculated using a Poisson-Schrödinger model.*

CV measurements of the HFET Sample B device were performed at 2 MHz to detect the electron channel at the AlGaN/GaN interface. For this purpose, the gate was biased and the source and drain were connected in parallel and grounded. Fig. 3 shows the measured room temperature CV profile of HFET Sample B. The typical shape was observed where the

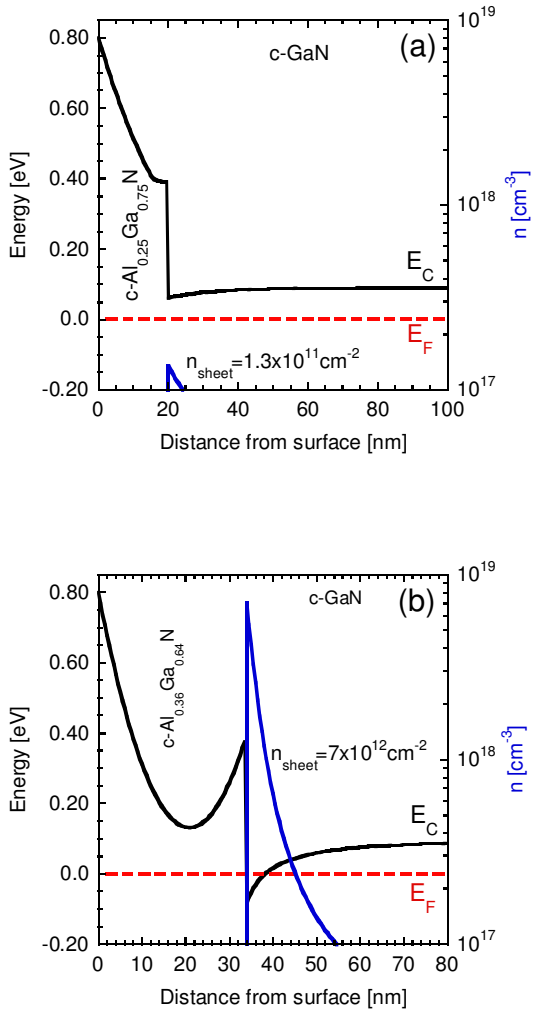

Figure 4. *Calculated conduction band edge and the electron concentration versus distance from surface at V_{GS}=0V for (a) Sample A and (b) Sample B.*

capacitance was found to be roughly constant when the electron channel was present, falling to smaller values once the electron channel had been depleted. The left-hand scale is the measured capacity which has been corrected for the parasitic parallel capacity of the contact pads (C_p=19.8 pF). The resulting gate capacity is plotted at the right hand-scale. The red dashed curve depicts calculated CV data using the self consistent Poisson-Schrödinger model [12] with a donor concentration of n=1.5×10^{18} cm^{-3} in cubic $Al_{0.36}Ga_{0.64}N$ and n=1×10^{17} cm^{-3} in cubic GaN.

The inset of Fig. 3 shows the apparent carrier density N_{CV} in HFET Sample B calculated from the CV characteristics using the following equations [14]:

$$N_{CV} = -\frac{C^3}{q\varepsilon\varepsilon_0 A^2}\frac{dV}{dC} \quad (1)$$

$$z_{CV} = \frac{\varepsilon\varepsilon_0 A}{C} \quad (2)$$

where z_{CV} is equal to the distance from the surface and A is the contact area. The resulting profile shows a carrier agglomeration at the AlGaN/GaN interface building an electron channel. The red dashed curve is the calculated carrier density using the self-consistent Poisson-Schrödinger model with a donor concentration of n_D=1.5×10^{18} cm^{-3} in cubic $Al_{0.36}Ga_{0.64}N$ and n_D=1×10^{17} cm^{-3} in cubic GaN.

Comparison of Normally on and Normally off HFET

We measured a much larger transconductance in Sample A than in Sample B. We believe that this is due to lower source and drain contact resistance in Sample A due to highly doping of GaN:Si cap layer with n=6×10^{19} cm^{-3}. In Sample B, the same metal contacts were evaporated on $Al_{0.36}Ga_{0.64}N$:Si with n=1.5×10^{18} cm^{-3}. As a results the source-to-drain current and therewith the transconductance of Sample B is limited by the contact resistance. The transconductance-to-shunt ratio is 0.22 in Sample A and 0.61 in Sample B measured at V_{DS}=10 V. Obviously the carbon doping of the cubic GaN buffer layer induces a reduction of the buffer leakage, but the optimum carbon concentration for insulating cubic GaN has still to be found.

To clarify the normally-off behavior of HFET Sample A and the normally-on behavior of HFET Sample B, band structures and electron density profiles were calculated for V_G=0V using a self-consistent Poisson-Schrödinger model. For the gate contact, a Schottky barrier of 0.8 eV

was assumed [4]. The simulation diagrams are shown for HFET Sample A (Fig. 4 (a)) and for HFET Sample B (Fig. 4 (b)). According to electrical measurements, the electron channel of Sample A is nearly depleted. To achieve a higher electron density at the AlGaN/GaN interface, a positive gate voltage has to be applied. In contrast to HFET Sample A, the electron channel is degenerate and conductive in HFET Sample B with a calculated sheet carrier concentration of $n_{sheet}=7\times10^{12}$ cm^{-2}. A negative gate voltage has to be applied to deplete the channel.

CONCLUSIONS

Non-polar *cubic AlGaN/GaN HFETs* were grown by plasma assisted MBE on free-standing 3C-SiC substrates. Both normally-on and normally-off HFETs were fabricated using contact lithography. A clear field effect with normally-on and normally-off behavior was measured at room temperature and verified by calculations using a self consistent Poisson-Schrödinger model. The electron channel at the cubic AlGaN/GaN interface was also detected by capacitance-voltage measurements. However the field effect was accompanied by a relative large shunt current through the GaN buffer which clearly demonstrates the need for further reduction of the buffer conductivity.

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REFERENCES

1. L. Shen, R. Coffie, D. Bultari, S.J. Heikmann, A. Chakraborthy, A. Chini, S. Keller, S.P. DenBaars, and U.K. Mishra, *IEEE Electron. Dev. Lett.* **25**, 7 (2004).
2. S. Rajan, P. Waltereit, C. Poblenz, S.J. Heikmann, D.S.Green, S.P. DenBaars, and U.K. Mishra, *IEEE Electron. Dev. Lett.* **25**, 247 (2004).
3. S. Haffouz, H. Tang, J.A. Bardwell, E.M. Hsu, J.B. Webb, and S. Rolfe, *Solid State Electron.* **49**, 802 (2005).
4. D.J. As, E. Tschumak, I. Laubenstein, R.M. Kemper, K. Lischka, *MRS. Symp. Proc. Vol*. **1108**, A01-02 (2009).
5. E. Tschumak, M.P.F. de Godoy, D.J. As, and K. Lischka, *Microelectronics Journal* **40**, 367 (2009).
6. J. Schörmann, S. Potthast, D.J. As, and K. Lischka, *Appl. Phys. Lett.* **90**, 041918 (2007).
7. E. Tschumak, J.K.N. Lindner, M. Bürger, K. Lischka, H. Nagasawa, M. Abe, and D.J. As, *phys. stat. sol. (c)* (2009) (to be published).
8. M. Kuroda, H. Ishida, T. Ueda, and T. Tanaka, J. Appl. Phys. **102**, 093703 (2007).
9. D.J. As, E. Tschumak, H. Pöttgen, O. Kasdorf, J.W. Gerlach, H. Karl, and K. Lischka, J. Crys. Growth **311**, 2039 (2009).
10. C. Poblenz, P. Waltereit, S. Rajan, S. Heikmann, U. K. Mishra, and J. S. Speck, J. Vac. Sci. Technol. **B 22(3),** 1145 (2004).
11. D.S. Green, U.K. Mishra, and J.S. Speck, J. Appl. Phys. **95**, 8456 (2004).
12. I.H. Tan, G. Snider, and E.L. Hu, J. Appl. Phys. **68**, 4071 (1990).