Superlattices and Microstructures 62 (2013) 260–268

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Comparative study on performance of cubic $Al_xGa_{1-x}N/GaN$ nanostructures MODFETs and MOS-MODFETs

Driss Bouguenna [a,*], A. Boudghene Stambouli [b], N. Mekkakia Maaza [b], A. Zado [c], D.J. As [c]

[a] Department of L.M.D Sciences of the Matter (SM), Faculty of Sciences & Technology, University of Mascara, 29000 Mascara, Algeria
[b] Electrical Engineering Laboratory of Oran, Department of Electronics, Faculty of Electrical & Electronics Engineering, University of Sciences & Technology of Oran, 31000 Oran, Algeria
[c] Department of Physics, Faculty of Science, University of Paderborn, Warburger Str. 100, 33095 Paderborn, Germany

ARTICLE INFO

Article history:
Received 28 June 2013
Received in revised form 29 July 2013
Accepted 2 August 2013
Available online 12 August 2013

Keywords:
Cubic $Al_xGa_{1-x}N/GaN$
Nanostructures
Device simulation
MODFET
MOS-MODFET
Next**nano**^{3}

ABSTRACT

We report some comparative results on cubic $Al_xGa_{1-x}N/GaN$ nanostructures MODFET and MOS-MODFET. The drain current characteristics of cubic $Al_xGa_{1-x}N/GaN$ MODFET and MOS-MODFET are simulated by changing the different device parameters such as Al content x and the cubic GaN buffer layer thickness using 2D next**nano**^{3} numerical simulation software. Drift–diffusion model has taken for simulating the proposed device. These results clearly indicate that the transistor simulation with 5 nm isolator SiO_2 layer thickness under the gate, Al content of $x = 25\%$ and 200 nm cubic GaN buffer layer thickness shows the tremendous I–V characteristics. Also, this structure shows an increase of the drain saturation current and a decrease in the threshold voltage. Moreover, our simulation results exhibited lower threshold voltage and higher drain current density of MOS-MODFET is a factor 30% higher than the same current of a conventional MODFET. The MODFET with 5 nm isolator SiO_2 layer thickness has been much better performance. To avoid current flow through the high conductive 3C-SiC substrate a 150 nm p-doped cubic GaN layer is deposited. A comparison between our experimental and simulation results are shown to be in good agreement for cubic $Al_{0.25}Ga_{0.75}N/GaN$ nanostructures MOS-MODFET. The demonstrated MOS-MODFET will be attractive for the next-generation microwave and high power switching application fields.

© 2013 Elsevier Ltd. All rights reserved.

* Corresponding author. Tel.: +213 458 64136; fax: +213 458 69314.
E-mail address: dbouguenna.um@gmail.com (D. Bouguenna).

0749-6036/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.spmi.2013.08.001

1. Introduction

Beside the impressive applications of group III nitrides in optoelectronics, the number of electronic devices based on wide gap III-nitrides is presently increasing. Due to the large band gap of GaN and AlN and their ternary compounds they are good candidates for high frequency and high power devices and tremendous research activities have been undertaken to grow multilayer group III-nitride stacks in still improving crystalline perfection. Most of these activities have been devoted to group III-nitrides with wurtzite (hexagonal) crystal structure.

However, group III-nitrides can also been grown in the less energetically favorable cubic (Zinc blende) structure, which due to the absence of built-in electric fields have some potential advantages over their hexagonal counterparts where built-in electric fields arising from spontaneous and piezoelectric polarization may set limits to the performance of some electronic devices. Thus the cubic structure may be advantageous for some device applications like normally-off field effect transistors. Also phonon scattering is lower in the cubic phase due to the higher crystallographic symmetry. As a result the mobility of electrons and holes in the cubic phase is expected to be larger than in hexagonal structures.

$Al_xGa_{1-x}N$/GaN hetero-junction field-effect transistors (HFETs) are of interest for high-power and high-frequency amplifiers. This is motivated by their potential in commercial and military applications, e.g. in communication systems, radar, wireless stations, high-temperature electronics and high-power solid-state switching. Currently, state of the art HFETs are fabricated on c-plane wurtzite $Al_xGa_{1-x}N$/GaN heterostructures. Their inherent polarization fields produce extraordinary large sheet carrier concentrations at the $Al_xGa_{1-x}N$/GaN hetero-interface which are advantageous for normally-on type transistors [1–3].

However, for switching devices and digital electronics field-effect transistors (FETs) with normally-off characteristics are desirable. It was discussed by Abe et al. [4] that the use of cubic III-nitrides would offer fabricating HFETs without parasitic polarization fields and with equal electrical properties for all gate orientations. Further, with cubic nitrides the same technology for the production of normally-on and normally-off devices can be applied. A first demonstration of a c-nitride HFET with normally-off characteristics with a threshold voltage of $V_{th} = 0.6$ V has recently been reported by Tschumak et al. [5]. The critical issue in the operation of this device was its high gate leakage current, which is undesirable for high power and low noise applications and severely reduces the device performance. Therefore, the use of metal/insulator layers instead of a Schottky gate, leading to the metal–insulator–semiconductor heterostructures field effect transistors (MIS-HFET), may improve the device characteristics [6,7]. Zado et al. [8] have fabricated different MIS structures on cubic GaN.

Moreover, $Al_xGa_{1-x}N$/GaN based MOS-HEMT structure was fabricated by Yue et al. [9] is used to validate the present model. For MOS devices, the gate insulator plays an important role, since the good quality dielectric layers would yield these devices with outstanding performances. **M**etal–**O**xide–**S**emiconductor **Mo**dulation-**D**oped-**F**ield-**E**ffect-**T**ransistor (**MOS-MODFET**) structure with a high quality insulating dielectric layer, inserted between the gate metal and $Al_xGa_{1-x}N$ is expected to offer reduced leakage current. Many dielectrics, including native oxide, SiO_2 [10] have been used as the insulating dielectric in $Al_xGa_{1-x}N$/GaN based MOS-MODFET [11].

However, the absence of spontaneous and piezoelectric fields in the cubic AlGaN/GaN system allows the fabrication of normally-on and normally-off heterojunction field-effect transistors (HFETs). However, the critical issue in the operation of the fabricated HFETs was the insufficient insulation of the gate contact. To improve the gate characteristics an insulating layer is required. Low interface trap density metal–insulator–semiconductor (MIS) interfaces are essential for high-power and high-frequency devices [12].

Therefore, the aim of our work is comparative study of the electrical characteristics of cubic $Al_xGa_{1-x}N$/GaN nanostructures MODFET [13] and MOS-MODFET switching devices using 2D next**nano³** numerical simulation software [14], changing the different device parameters such as the Al content x and the cubic GaN buffer layer thickness at $V_{DS} = 0$ V for the output characteristics and at $V_{GS} = 0$ V for the transfer characteristics of the MODFET and MOS-MODFET. $Al_xGa_{1-x}N$/GaN

MOS-MODFET has received great attention due to their lower gate leakage current and larger gate voltage swing compared to the conventional Schottky gate HFETs (SG-HFET) [15–17].

Furthermore, we have assumed 5 nm gate oxide thicknesses. The stability of the device parameters determines the maximum acceptable operating voltage below 5 nm of gate oxide [18–22] with $x = 25\%$ Al content of the barrier layer and 200 nm of cubic GaN buffer layer thickness have been improving the performances of cubic $Al_xGa_{1-x}N$/GaN nanostructures MODFET, with decreasing of buffer leakage by thinner c-GaN buffer layer. However, this device offered high parallel conductivity through the thick c-GaN buffer [23]. This is decreasing the trap states at the interface of hetero-structures results the reduction scattering processes, whereas decreasing the parasite source resistance to avoid gate leakage current and current collapse. Thus, our simulation results shown that the MOS-MODFET superior performance to that of conventional MODFET, compared with the results similar which obtained by Narihiko Maeda et al. for the design of insulator/$Al_xGa_{1-x}N$ structures in MOS $Al_xGa_{1-x}N$/GaN HFET for higher device performance [24] and by Ki-Yeol Park et al. for the comparative study on $Al_xGa_{1-x}N$/GaN HFET and MIS-HFET [25] confirms the validity of the proposed model. Moreover, we report on comparative study on cubic $Al_xGa_{1-x}N$/GaN nanostructures based MODFET and MOS-MODFET.

2. Simulation results

In this work, we have simulated the *I–V* characteristics of two different devices such as cubic $Al_xGa_{1-x}N$/GaN nanostructures MODFET and MOS-MODFET by using 2D next**nano³** numerical simulation software. We have assumed in our calculations 10 μm for a long the devices structures with 2 μm gate length.and without strain.

2.1. Design considerations

Fig. 1 shows the device structure of cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET with *p*-type doping sample consisting of 150 nm *p*-doped (UID) cubic GaN buffer layer (doping concentration of $N_A = 1 \times 10^{17}$ cm^{-3}), where deposited on the 3C-SiC substrate in (001) direction. The 3C-SiC substrate is highly doped with a free electron concentration of 3×10^{18} cm^{-3}. On top 50 nm of the UID cubic GaN buffer layer with a net doping concentration of $N_D = 1 \times 10^{17}$ cm^{-3}, followed by the growth of a 4 nm of UID cubic $Al_xGa_{1-x}N$ spacer layer with $N_D = 5 \times 10^{17}$ cm^{-3}, 6 nm of cubic $Al_xGa_{1-x}N$: Si with $N_D = 5 \times 10^{18}$ cm^{-3}, 10 nm of UID cubic $Al_xGa_{1-x}N$ with $N_D = 5 \times 10^{17}$ cm^{-3}, and with 5 nm of

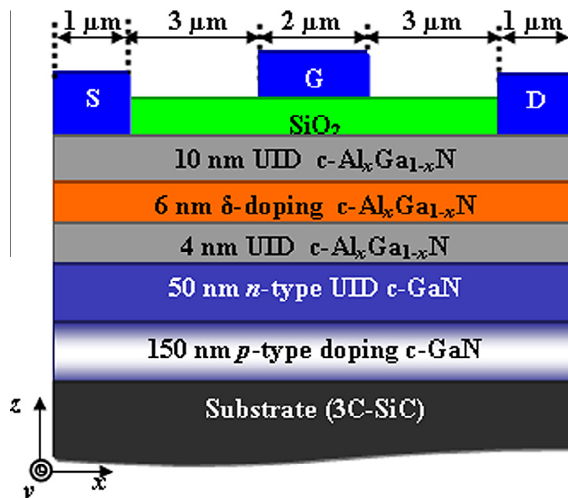

Fig. 1. Schematic cross-section of cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET with p-type doping.

the SiO_2 insulator thickness. To avoid current flow through the high conductive 3C-SiC substrate a 150 nm *p*-doped cubic GaN layer is deposited. This results in two *p*–*n* junctions at the SiC/*p*-GaN, and the *p*-GaN/*n*-GaN interfaces forming high insulating layers. Finally, the MOS-MODFET sample device has simulated using two-dimensional numerical simulation next**nano³** software for the calculations of the electrical output and transfer characteristics.

2.2. Results and discussion

For the validation of our model, we present comparison between the simulation and experimental results. Fig. 2 shows the experimental data and simulation results of the transfer characteristics of cubic $Al_{0.25}Ga_{0.75}N$/GaN nanostructures MOS-MODFET were compared, for the purpose of calibrating and validating the simulation results. The model parameters is adjusted to get a perfect matching between experimental and simulation results is shown in Fig. 2 for the transfer characteristics of cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET at $V_{DS} = 0$ V and at room temperature. After matching is done, the model is then applied for simulating our model proposed of cubic $Al_{0.25}Ga_{0.75}N$/GaN nanostructures MOS-MODFET. The numerical simulator uses drift–diffusion model to solve the Poisson's equation self-consistently with carrier continuity equation. We have assumed the mobility-model-simba-2, if the exponents kappa^{n,p} are temperature dependent then this equation is called Canali model (with $\mu^{n,p}$ as the low field mobility) [14] with suitable modifications to precisely capture the non-equilibrium carrier transport:

$$\mu^{p,n}(\vec{E}) = \frac{\mu^{p,n}}{\left[1 + \left(\mu^{p,n} \frac{|\vec{E}|}{v_0^{p,n}}\right)^{\kappa^{p,n}}\right]^{1/\kappa^{p,n}}} \tag{1}$$

The device transfer characteristics are shown in Fig. 2, a good matching between the experimental and simulation results of the transfer characteristics at $V_{DS} = 0$ V with the simulation results, thus the model is validated, extensive simulation of cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET is then has been done.

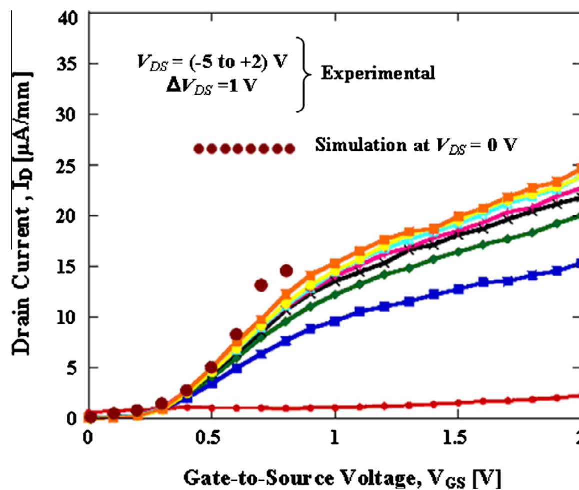

Fig. 2. (Color lines) represent transfer characteristics of cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET fabricated at room temperature. The dotted brown line represents calculated transfer characteristics at VDS = 0 V. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

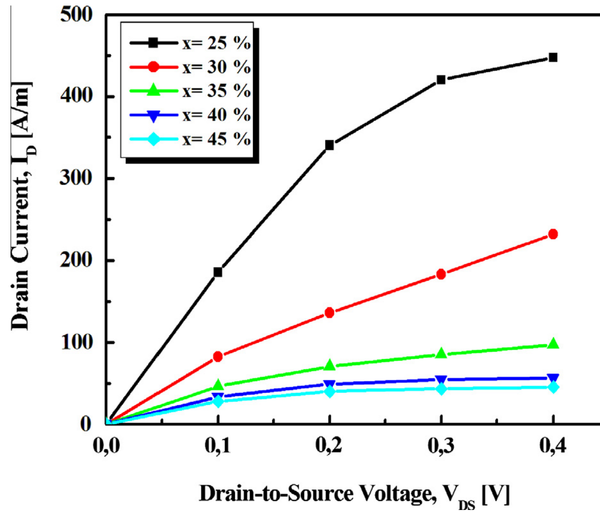

Fig. 3. The electrical output characteristics of cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET with different Al content are calculated at room temperature.

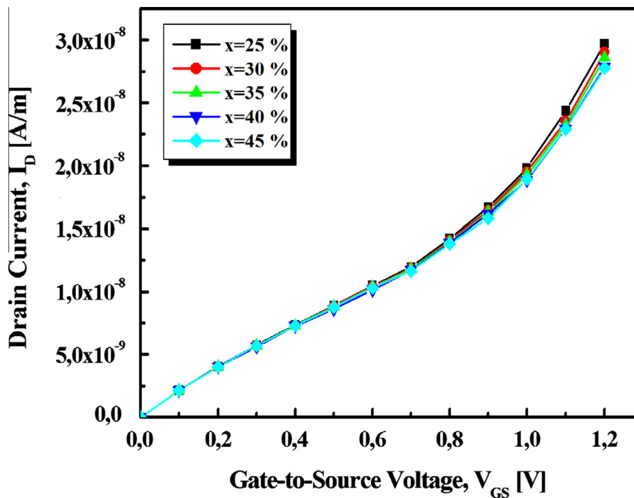

Fig. 4. The electrical transfer characteristics of cubic $Al_xGa_{1-x}N$/GaN nanostructures based MOS-MODFET at different Al content are calculated at room temperature.

2.2.1. Variation in Al content x within the $Al_xGa_{1-x}N$ barrier layer

Figs. 3 and 4 show the simulated electrical characteristics of the cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET, for different values of Al content x in the cubic $Al_xGa_{1-x}N$ barrier layer, (25%, 30%, 35%, 40%, and 45%) are calculated at room temperature. At $x = 25\%$ (black line), the MOS-MODFET reaches a maximum saturation drain current density is shown in Fig. 3. On the other hand, Fig. 4 shows the electrical transfer characteristics at $V_{DS} = 0$ V, where the MOS-MODFET reaches a low value of threshold voltage at $x = 25\%$. Thus, the current flowing in the device depends strongly on the Al contents of the top layer. This is essentially due to increase in the current drain saturation of the normally-off MOS-MODFET.

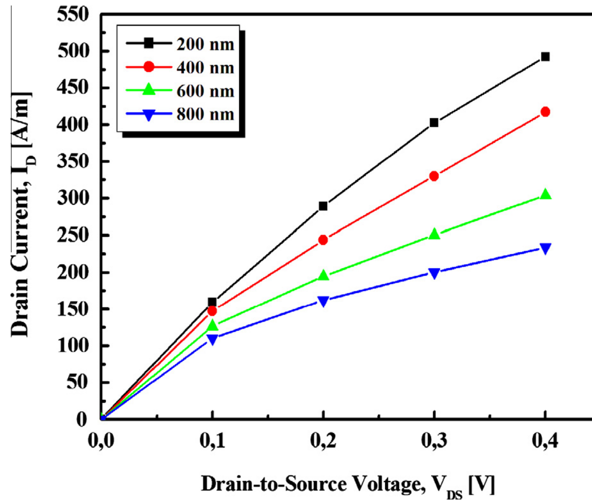

Fig. 5. The current–voltage characteristics of cubic $Al_{0.25}Ga_{0.75}N$/GaN nanostructures MOS-MODFET with different thickness of cubic GaN buffer are calculated at VGS = 0 V and at room temperature.

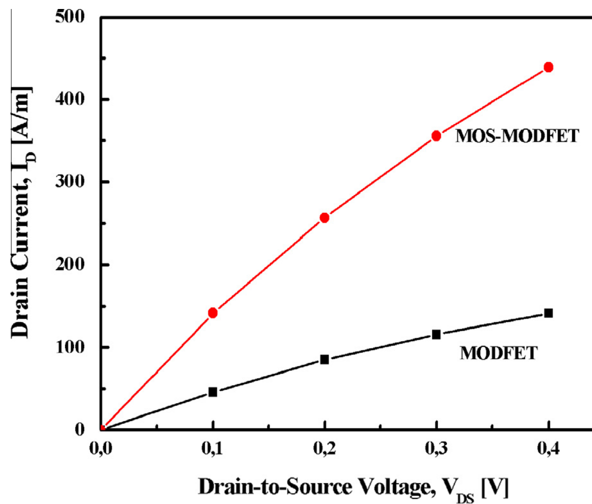

Fig. 6. The electrical output characteristics of cubic $Al_{0.25}Ga_{0.75}N$/GaN nanostructures MODFET and MOS-MODFET are calculated at room temperature.

2.2.2. Variation in thickness of cubic GaN buffer layer

Fig. 5 shows the simulated I_D–V_{DS} characteristics of the model of cubic $Al_{0.25}Ga_{0.75}N$/GaN nanostructures MOS-MODFET with different thickness of cubic GaN buffer layer varied from (200 to 800) nm in a step of 200 nm are calculated at V_{GS} = 0 V. Our simulation results indicate that the fabrication of the MOS-MODFET nanostructures by using a thinner cubic GaN buffer layer successfully decreasing the buffer leakage current, which is critical to obtain a maximum drain current. Thus, the current flowing in the device increases with reduction of the impurity scattering in the buffer layer, thereby increasing electron mobility within the channel and yielding a high device transconductance.

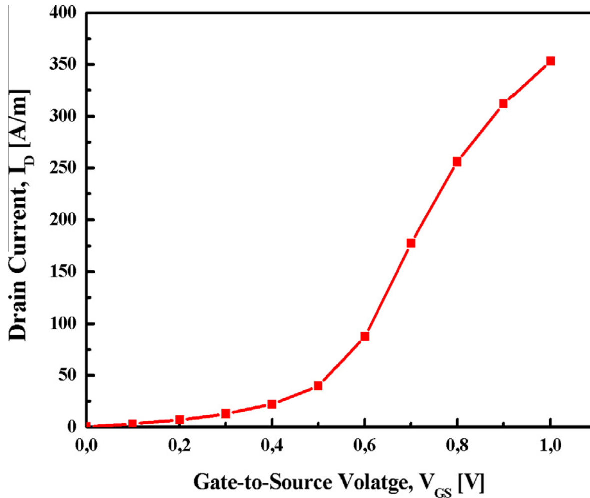

Fig. 7. The electrical transfer characteristics of cubic $Al_{0.25}Ga_{0.75}N/GaN$ nanostructures MODFET are calculated at room temperature.

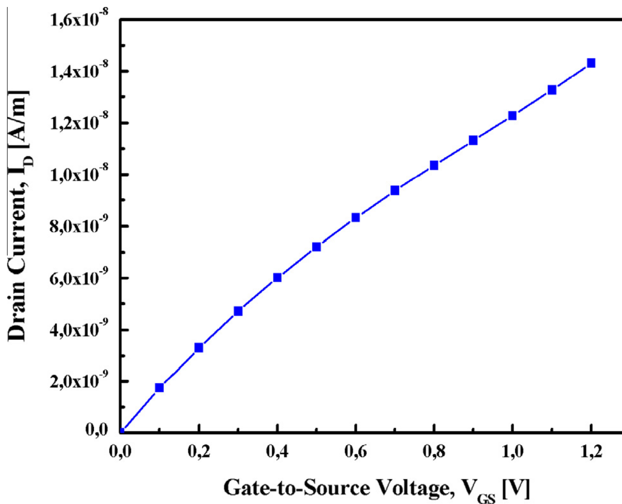

Fig. 8. The electrical transfer characteristics of cubic $Al_{0.25}Ga_{0.75}N/GaN$ nanostructures MOS-MODFET are calculated at room temperature.

2.2.3. Comparative study on device characteristics of cubic $Al_xGa_{1-x}N/GaN$ nanostructures MODFET and MOS-MODFET

Fig. 6 shows the comparison of electrical output characteristics when the gate bias V_{GS} is at 0 V. Cubic $Al_{0.25}Ga_{0.75}N/GaN$ nanostructures MODFET with and without SiO_2 gate insulator have I_{DSS} of 439 and 141 A/m, respectively at $V_{DS} = 0.4$ V. This result may be attributed to the increase in effective carrier concentration in the channel in MODFET with insulating gate layer. From a comparison of the saturation currents of this device, the different influences of the insulating cap layer become evident. Compared with a free-surface of MODFET without SiO_2 gate insulator, the structures with an insulating cap layer have a lower surface-state density that reduces the surface-related depletion

effects. Moreover, the structure with a high-resistively capping layer reduces the electronic density of states at the interface with cubic $Al_{0.25}Ga_{0.75}N$. It is clear from the figure that for same value of gate and for same values of drain bias, the drain current is higher for $Al_{0.25}Ga_{0.75}N$/GaN MOS-MODFET than that a conventional counterpart. This leads to a reduction of surface-related depletion of the channel layer and increases the sheet carrier concentration [26] by about 32%. Figs. 7 and 8 show the transfer characteristics of the MODFET and MOS-MODFET, respectively. The gate current of MOS-MODFET is smaller than that of a conventional MODFET and therefore present high device transconductance. Our simulation results shown that the electrical performance can be enhanced through the surface gate insulation.

3. Conclusions

The evaluation of the drain current characteristics of cubic $Al_xGa_{1-x}N$/GaN based MOS-MODFET has been presented to compare the device performance. The proposed model design can easily be used to predict the characteristics of MODFET as well. The MOS-MODFET structure shows clearly an advantage over their MODFET counterparts in terms of gate voltage swing and higher saturation currents. With 5 nm isolator SiO_2 layer thickness under the gate, Al content $x = 25\%$ of cubic $Al_xGa_{1-x}N$ layer and a thinner cubic GaN buffer layer successfully decreasing the buffer leakage current, which is critical to obtain a maximum drain current. The simulation results suggest that with a lower thick of SiO_2 gate insulator exhibited excellent DC characteristics of cubic $Al_xGa_{1-x}N$/GaN FET. The MODFET with 5 nm thick SiO_2 insulator has much better performances. To avoid current flow through the high conductive 3C-SiC substrate a 150 nm *p*-doped cubic GaN layer is deposited. This results in two *p*–*n* junctions at the 3C-SiC/*p*-GaN, and the *p*-GaN/*n*-GaN interfaces forming high insulating layers. Our simulation results have exhibited a maximum saturation drain current with Al content $x = 25\%$ at the gate voltage $V_{GS} = 0$ V of SiO_2/cubic $Al_xGa_{1-x}N$/GaN nanostructures MOS-MODFET. This model provides a valuable tool for design, optimization, and performance prediction of microwave power devices and demonstrates clear superiority of MOS-MODFET over MODFET for application of optical devices.

Acknowledgments

The work is a joint collaboration between the group of Physics and Technology of Optoelectronic Semiconductors at University of Paderborn, Germany and Laboratory of Electrical Engineering at University of Sciences and Technology of Oran, Algeria.

References

[1] S. Rajan, P. Waltereit, C. Poblenz, S.J. Heikman, D.S. Green, J.S. Speck, U.K. Mishra, Power performance of AlGaN/GaN HEMTs grown on SiC by plasma-assisted MBE, IEEE Electron. Dev. Lett. 25 (May 2004) 247–249.
[2] S. Haffouz, H. Tang, J.A. Bardwell, E.M. Hsu, J.B. Webb, S. Rolfe, AlGaN/GaN field effect transistors with C-doped GaN buffer layer as an electrical isolation template grown by molecular beam epitaxy, Solid-State Electron. 49 (5) (May 2005) 802–807.
[3] Y.C. Choi, J. Shi, M. Pophristic, M.G. Spencer, L.F. Eastman, C-doped semi-insulating GaN HFETs on sapphire substrates with a high breakdown voltage and low specific on-resistance, J. Vac. Sci. Technol. B 25 (6) (Oct 2007) 1836–1842.
[4] M. Abe, H. Nagasawa, S. Potthast, J. Fernandez, J. Schörmann, D.J. As, K. Lischka, Cubic GaN/AlGaN HEMTs on 3C-SiC substrate for normally-off operation, IEICE Trans. Electron. 89 (7) (Jan 2006) 1057–1063.
[5] E. Tschumak, R. Granzer, J.K.N. Lindner, F. Schwierz, K. Lischka, H. Nagasawa, M. Abe, D.J. As, Nonpolar cubic AlGaN/GaN heterojunction field-effect transistors on Ar^+ implanted 3C–SiC (001), Appl. Phys. Lett. 96 (25) (Jun 2010) 3501–3503.
[6] V. Adivarahan, J. Yang, A. Koudymov, G. Simin, M. Asif Khan, Stable CW operation of field-plated GaN/AlGaN MOSHFETs at 19 W/mm, IEEE Electron. Dev. Lett. 26 (8) (Aug 2005) 535–537.
[7] R.B. Gila, F. Ren, C.R. Abernathy, Novel insulators for gate dielectrics and surface passivation of GaN-based electronic devices, Mater. Sci. Eng.: R 44 (6) (Sep 2001) 151–184.
[8] A. Zado, K. Lischka, D.J. As, Electrical properties of MBE grown Si_3N_4 cubic GaN MIS structures, Phys. Stat. Sol. C 9 (3-4) (Mar 2012) 1088–1091.
[9] Yue. Yuanzheng, Hao. Yue, Feng. Qian, et al, GaN MOS-HEMT using ultra-thin Al_2O_3 dielectric grown by atomic layer deposition, Chin. Phys. Lett. 24 (8) (Aug 2007) 2419–2422.
[10] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, M. Umeno, Investigations of SiO_2/*n*-GaN and Si_3N_4/*n*-GaN insulator-semiconductor interfaces with low interface state density, Appl. Phys. Lett. 73 (6) (Aug 1998) 809–811.
[11] S.M. Sze, Semiconductor Devices-Physics & Technology, Wiley, 0471333727, New York, 2002.

[12] A. Zado, J. Gerlach, D.J. As, Low interface trapped charge density in MBE in situ grown Si3N4 cubic GaN MIS structures, Semicond. Sci. Technol. 27 (3) (2012).
[13] Driss. Bouguenna, A. Boudghene Stambouli, A. Zado, D.J. As, N. Mekkakia Maaza, 2D simulations of current–voltage characteristics of cubic $Al_xGa_{1-x}N$/GaN modulation doped hetero-junction field effect transistor structures, Sci. Acad. Pub. Electr. Electron. Eng. 2 (5) (Oct 2012) 309–315.
[14] http://www.wsi.tum.de/nextnano[3] and http://www.nextnano.de.
[15] Wang Chong, Ma Xiaohua, Feng Qian, et al, Development and characteristics analysis of recessed-gate MOS HEMT, J. Semicond. 30 (5) (May 2009) 054002–054005.
[16] D. Gregusova, R. Stoklas, K. Cico, et al, AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect transistors with 4 nm thick Al_2O_3 gate oxide, Semicond. Sci. Technol. 22 (8) (Aug 2007) 947–951.
[17] N. Maeda, M. Hiroki, N. Watanabe, et al, Insulator engineering in GaN-based MIS HFETs, Proc. SPIE, Gallium Nitride Mater. Dev. II 6473 (Feb 2007) 647316.
[18] Moongyu Jang, Yarkyeon Kim, Jaeheon Shin, Seongjae Lee, Kyoungwan Park, A 50-nm-gate-length erbium-silicided n-type Schottky barrier metal-oxide-semiconductor field-effect transistor, Appl. Phys. Lett. 84 (5) (2004).
[19] Moongyu Jang, Yarkyeon Kim, Jaeheon Shin, Seongjae Lee, Kyoungwan Park, Novel properties of erbium-silicided n-type schottky barrier metal-oxide-semiconductor field-effect transistors, J. Semicond. Technol. Sci. 4 (2) (Dec 2004) 94–99.
[20] Seongjae. Lee, Moongyu. Jang, Yarkyeon. Kim, Myungsim. Jeon, Kyoungwan. Park, Schottky barrier metal-oxide-semiconductor field-effect transistors for nano-regime applications, Electron. Mater. Lett. 1 (1) (Sep 2005) 27–29.
[21] K. Okuyama, K. Yoshikawa, H. Sunami, Control of subthreshold characteristics of narrow-channel silicon-on-insulator n-type metal-oxide-semiconductor transistor with additional side gate electrodes, Jpn. J. Appl. Phys. 46 (4B) (2007) 24.
[22] K.F. Schuegraf, D. Park, C. Hu, Reliability of thin SiO_2 at direct-tunneling voltages, IEEE Electron. Dev. Meet. 609–612 (Dec 1994) 11–14.
[23] E. Tschumak, Cubic AlGaNGaN hetero-junction field-effect transistors with normally-on and normally-off characteristics, in: AIP Conf. Proc, vol. 1292, October 8–10, 2010. pp. 159–164.
[24] Narihiko Maeda, Masanobu Hiroki, Takatomo Enoki, Takashi Kobayashi, Design of insulator/AlGaN structures in MIS AlGaN/GaN HFETs for higher device performance, Proc. SPIE 7216 (Feb 2009). 721605-1.
[25] Ki-Yeol Park, Hyun-Ick Cho, Hyun-Chul Choi, Jung-Hee Lee, Comparative study on AlGaN/GaN HFETs and MIS-HFETs, J. Kor. Phys. Soc. 45 (2004) S898–S901.
[26] C.J. Kao, M.C. Chen, C.J. Tun, G.C. Chi, J.K. Sheu, W.C. Lai, M.L. Lee, F. Ren, S.J. Pearton, Comparison of low-temperature GaN, SiO_2, and SiN_x as gate insulators on AlGaN/GaN heterostructure field-effect transistors, J. Appl. Phys. 98 (6) (2005) 064506.