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# Non-polar cubic AlGaN/GaN HFETs grown by MBE on $Ar^+$ implanted 3C-SiC (001)

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The growth of cubic group III-nitrides is a direct way to eliminate polarization effects, which inherently limit the fabrication of normally-off heterojunction field-effect transistors (HFETs) in GaN technology. HFET structures were fabricated of non-polar cubic AlGaN/GaN hetero layers grown by plasma assisted molecular beam epitaxy (MBE) on free standing 3C-SiC (001). The electrical insulation of 3C-SiC was realised by Ar+ implantation before c-AlGaN/GaN MBE. The structural properties of the epilayers were studied by high-resolution x-ray diffraction (HRXRD). HFETs with normally-off and normally-on characteristics were fabricated of cubic AlGaN/GaN. Capacitance-voltage (CV) characteristics of the gate contact were performed to detect the electron channel at the c-AlGaN/GaN hetero interface.



**1 Introduction** AlGaN/GaN hetero junction field-effect transistors are presently of major interest for electronic devices, in particular, for high-power and high-frequency amplifiers. This is motivated by the potential for commercial and military application, e. g. in communication systems, radar, wireless stations, high-temperature electronics and high-power solid-state switching [1, 2]. Currently, state of the art AlGaN/GaN HFETs are fabricated of the c-plane surface of the stable wurzite (hexagonal) crystal structure with inherent spontaneous and piezoelectric polarization fields which produce extraordinary high sheet carrier concentrations at the hetero interface. Therefore, all these devices are of the normally-on type [3, 4]. However, for switching devices normally-off field effect transistors (FETs) are necessary. Several groups reported on AlGaN/GaN HFETs with normally-off operations. Sugiura et al. [5] fabricated a normally-off MOSFET with $HfO_2$ gate oxide. Ito et al. [6] used the polarization induced field in a thin InGaN cap layer on a conventional AlGaN/GaN high electron mobility transistor (HEMT) structure to enhance the conduction band of the AlGaN/GaN interface. Kuroda et al. [7] realized a non-polar *a*-plane AlGaN/GaN HFET with nearly normally-off operation in which the threshold voltage is only -0.5 V. However, the growth of cubic group III-nitrides would provide a direct way to fabricate HFETs without undesirable parasitic piezoelectric and polarization effects using the same technologies for normally-on and normally-off devices.

In this paper, non-polar cubic AlGaN/GaN hetero structures grown on free standing $Ar^+$ implanted 3C-SiC are analysed as a possible solution for normally-on and normally-off HFETs.

**2 Experiment and discussion** For the epitaxy of cubic AlGaN/GaN hetero structures, freestanding $Ar^+$ implanted 3C-SiC was used. Previous to the $Ar^+$ implantation, the carrier concentration in the 3C-SiC substrate of $n=2\times10^{18}$ $cm^{-3}$ was measured by Hall effect. A three energy implantation with Ar ions at doses of $6\times10^{14}$ $cm^{-2}$ at 160 keV, $2.4\times10^{14}$ $cm^{-2}$ at 80 keV and $1.2\times10^{14}$ $cm^{-2}$ at 40 keV was used to form a damage layer near the surface. We showed that this damage acts as insulation layer [8]. Reflection high energy electron diffraction (RHEED) was used to monitor the crystalline nature of the sample surface.

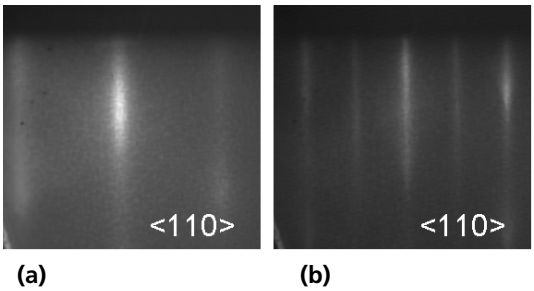


**Figure 1** RHEED pattern of (a) 3C-SiC after $Ar^+$ implantation and (b) cubic GaN after 600 nm growth on $Ar^+$ implanted 3C-SiC.

Figure 1 shows streaky RHEED patterns of $Ar^+$ implanted 3C-SiC (a) and of 600 nm cubic GaN (c-GaN) grown on this substrate (b) revealing a two dimensional surface condition.

Cubic $Al_xGa_{1-x}N$/GaN hetero structures were grown in a Riber 32 system by plasma-assisted molecular beam epitaxy. Prior to growing process, the substrate was chemically etched by organic solvents and buffered oxide etching (BOE). In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness, coverage of one monolayer Ga was established during growth [9]. The substrate temperature was 720°C and the growth rate was 115 nm/h.

Two different cubic $Al_xGa_{1-x}$ N/GaN hetero structures (Sample A and Sample B) with similar crystalline properties were investigated. The full width at half maximum (FWHM) of the cubic GaN (002) rocking curve was 25 arcmin. The RMS roughness of the surface measured by AFM in a 5×5 $\mu m^2$ scan was 5 nm. In both samples, the cubic $Al_xGa_{1-x}N$ was pseudomorphically strained on the cubic GaN, indicated by the position of the cubic $Al_{0.36}Ga_{0.64}N$ reflex relative to the cubic GaN reflex of Sample B shown in Fig. 2.

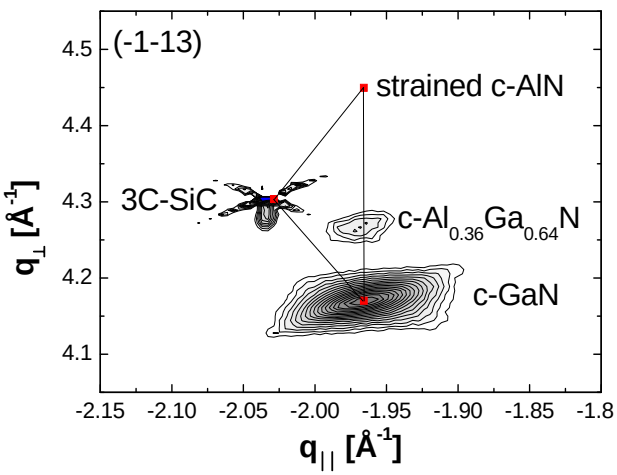


**Figure 2** Reciprocal space map of the (-1-13) reflection of cubic GaN and AlGaN epilayer.

**2.1 HFET Sample A with normally-off characteristics** Sample A consists of 600 nm unintentionally doped (UID) cubic GaN followed by 3 nm UID cubic $Al_{0.25}Ga_{0.75}N$ spacer layer, 2 nm cubic $Al_{0.25}Ga_{0.75}N$:Si and 15 nm UID cubic $Al_{0.25}Ga_{0.75}N$. The carrier concentration of the Si doped AlGaN layer is $n$=4.5×$10^{18}$ $cm^{-3}$. A 5 nm thick heavily silicon doped cubic GaN:Si cap with a carrier concentration of $n$=6×$10^{19}$ $cm^{-3}$ was grown on top of the sample.

For the source and drain contacts, Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated on GaN:Si and annealed at 850°C for 30 s in nitrogen environment to form ohmic source and drain contacts. Then, mesa insulation was performed with $SiCl_4$ reactive ion etching (RIE) down to the substrate. For the gate contact, the GaN:Si cap layer was removed using RIE with $SiCl_4$. The gate was fabricated by evaporation of Pd/Ni/Au (15 nm/15 nm/50 nm) and a subsequent annealing process at 400°C for 10 min. The device had a gate length of 2 µm, a gate width of 25 µm and a source-to-drain spacing of 8 µm. 250 nm of $SiO_2$ was deposited around the device to insulate the contact pads electrically.

The room temperature DC drain current-voltage curves with gate-to-source voltages from -1 V to + 5V of HFET Sample A are displayed in Fig. 3. The threshold voltage of this device is +0.7 V measured at $V_{DS}$=10 V by extrapolation of the transconductance curve (not shown here). This indicates a normally-off device characteristics, however, the drain-to-source current at $V_G$ = 0 V is relatively large due to the high conductivity of c-GaN buffer layer. The inset shows the measurement data adjusted by the shunt current. A maximum drain-to-source current of 6.5 mA/mm was observed when a gate voltage of +5 V was applied.

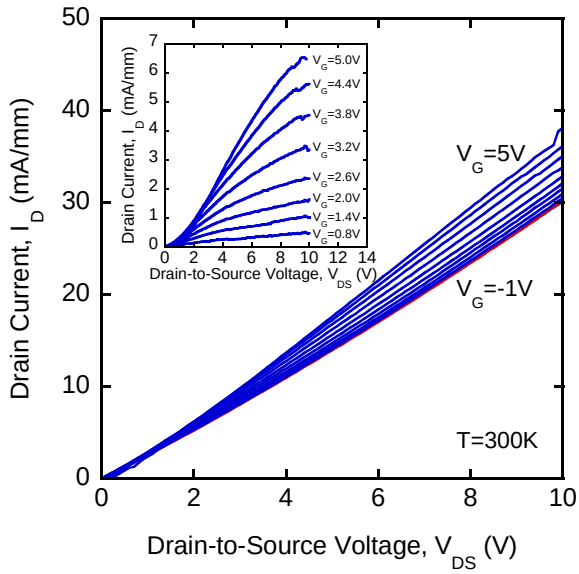


**Figure 3** Static output characteristics of the HFET A. The inset shows the same measurement curves corrected for the drain current at $V_{GS}$=-1 V.

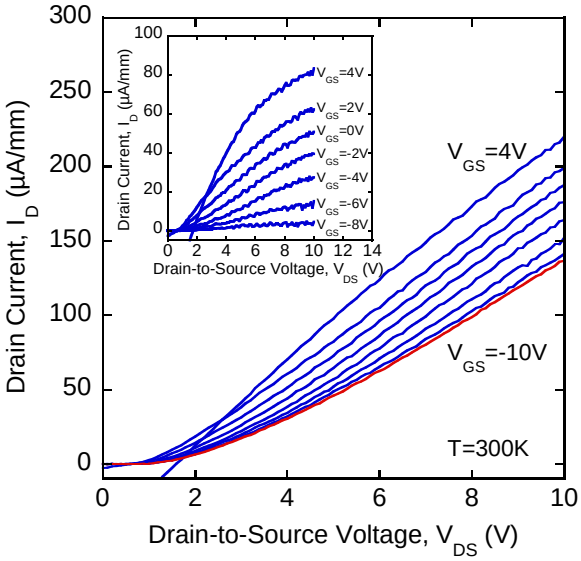


**Figure 4** Static output characteristics of the HFET B. The inset shows the same measurement curves corrected for the drain current at $V_{GS}$=-10 V.

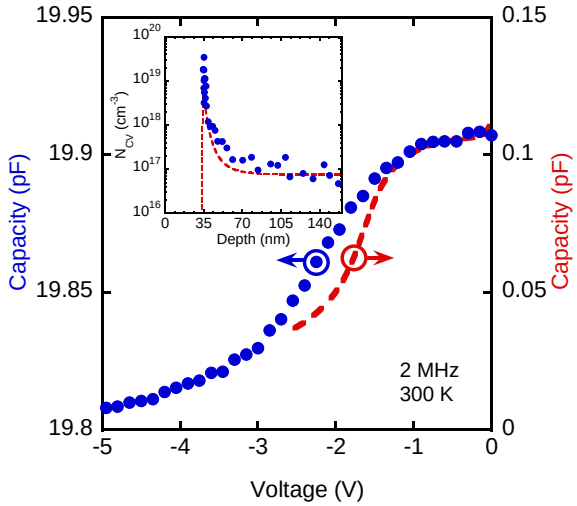


**Figure 5** CV characteristics of HFET B measured on the gate contact at 2 MHz confirming the presence of an electron channel at the AlGaN/GaN interface. The inset shows a carrier density profile $N_{CV}$. The red dashed lines are CV curves calculated using a Poisson-Schrödinger model.

**2.2 HFET Sample B with normally-on characteristics** To minimize the shunt current through the cubic GaN buffer layer, carbon doping using $CBr_4$ [10-12] was tested in Sample B. Sample B consists of a 60 nm UID cubic GaN nucleation layer followed by 580 nm carbon doped cubic GaN:C. For the carbon doping a $CBr_4$ beam equivalent pressure (BEP) of $1\times10^{-6}$ mbar was used. A 34 nm thick homogeneously doped $Al_{0.36}Ga_{0.64}N$:Si cap with a carrier concentration of $n=1.5\times10^{18}$ cm$^{-3}$ was grown on top of the sample.

For the source and drain contacts, 10 nm of the $Al_{0.36}Ga_{0.64}N$ top layer were removed by reactive ion etching (RIE) with $SiCl_4$. After that Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated and annealed at 850 °C for 30 s in a nitrogen environment. Then the Pd/Ni/Au gate contact was fabricated as described for HFET A. The device geometry was the same as for HFET Sample A.

The room temperature output characteristics of HFET Sample B are depicted in Fig. 4. The gate-to-source voltage was varied between -10 V and +4 V. Apart from the shunt current through the 3C-SiC substrate and GaN:C buffer layer (red curve), a clear field effect with normally-on characteristics is measured in this sample. The inset shows the same measurement data adjusted by the shunt current. The measurements of the source and drain contact resistance showed a slight non ohmic behaviour which limited the absolute current through the device. Therefore, the source-to-drain current difference between $V_G$=-10 V and $V_G$=+4 V was 80 µA/mm only. At high positive gate voltages, an additional gate leakage is observed at low source-to-drain voltages. So, the drain current at +4 V gate voltage is reduced by the gate leakage.

CV measurements of the HFET Sample B device were performed at 2 MHz to detect the electron channel at the AlGaN/GaN interface. For this purpose, the gate was biased and the source and drain were connected in parallel and grounded. Figure 5 shows the measured room temperature CV profile of HFET Sample B. The typical shape was observed where the capacitance was found to be roughly constant when the electron channel was present, falling to smaller values once the electron channel had been depleted. The left-hand scale is the measured capacity which has been corrected for the parasitic parallel capacity of the contact pads ($C_p$=19.8 pF). The resulting gate capacity is plotted at the right hand-scale. The red dashed curve depicts calculated CV data using the self consistent Poisson-Schrödinger model [13] with a donor concentration of $n=1.5\times10^{18}$ cm$^{-3}$ in cubic $Al_{0.36}Ga_{0.64}N$ and $n=1\times10^{17}$ cm$^{-3}$ in cubic GaN.

The inset of Fig. 5 shows the apparent carrier density $N_{CV}$ in HFET Sample B calculated from the CV characteristics using the following equations [14]:

$$N_{CV} = -\frac{C^2}{e\varepsilon\varepsilon_0 A^2}\frac{dV}{dC} \quad (1)$$

$$z_{CV} = \frac{\varepsilon\varepsilon_0 A}{C} \quad (2)$$

where $z_{CV}$ is equal to the distance from the surface and $A$ is the contact area. The resulting profile shows a carrier agglomeration at the AlGaN/GaN interface building an electron channel. The red dashed curve is the calculated carrier density using the self-consistent Poisson-Schrödinger model with a donor concentration of $n_D=1.5\times10^{18}$ cm$^{-3}$ in cubic $Al_{0.36}Ga_{0.64}N$ and $n_D=1\times10^{17}$ cm$^{-3}$ in cubic GaN.

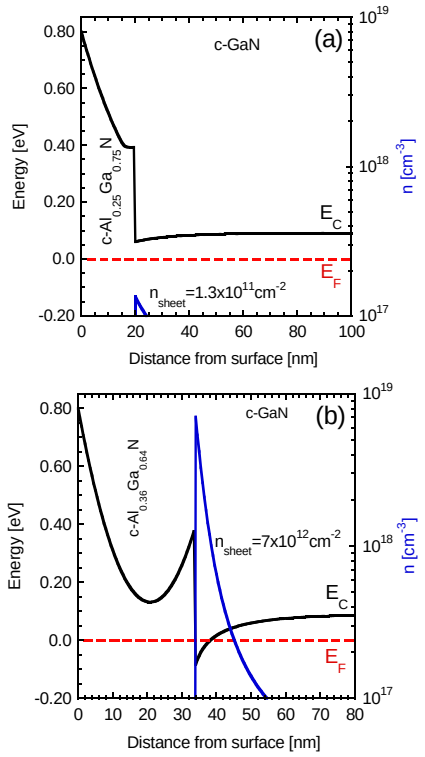


**Figure 6** Calculated conduction band edge and the electron concentration versus distance from surface at $V_{GS}$=0V for (a) Sample A and (b) Sample B.

**2.3 Comparison of sample A and sample B** We measured a much larger transconductance in Sample A than in Sample B. We believe that this is due to lower source and drain contact resistance in Sample A due to highly doping of GaN:Si cap layer with $n$=6×10$^{19}$ cm$^{-3}$. In Sample B, the same metal contacts were evaporated on $Al_{0.36}Ga_{0.64}N$:Si with $n$=1.5×10$^{18}$ cm$^{-3}$. As a results the source-to-drain current and therewith the transconductance of Sample B is limited by the contact resistance.

The transconductance-to-shunt ratio is 0.22 in Sample A and 0.61 in Sample B measured at $V_{DS}$ = 10 V. Obviously the carbon doping of the cubic GaN buffer layer induces a reduction of the buffer leakage, but the optimum carbon concentration for insulating cubic GaN has still to be found.

To clarify the normally-off behaviour of HFET Sample A and the normally-on behaviour of HFET Sample B, band structures and electron density profiles were calculated for $V_G$ = 0 V using a self-consistent Poisson-Schrödinger model. For the gate contact, a Schottky barrier of 0.8 eV was assumed [15]. The simulation diagrams are shown for HFET Sample A (Fig. 6(a)) and for HFET Sample B (Fig. 6(b)). According to electrical measurements, the electron channel of Sample A is nearly depleted. To achieve a higher electron density at the AlGaN/GaN interface, a positive gate voltage has to be applied.

In contrast to HFET Sample A, the electron channel is degenerate and conductive in HFET Sample B with a calculated sheet carrier concentration of $n_{sheet}$=7×10$^{12}$ cm$^{-2}$. A negative gate voltage has to be applied to deplete the channel.

**3 Conclusions** Free standing Ar$^+$ implanted 3C-SiC was used as substrate for c-AlGaN/GaN molecular beam epitaxy. A clear field effect with normally-on and normally-off behaviour was measured at room temperature and verified by calculations using a self consistent Poisson-Schrödinger model. The electron channel at the cubic AlGaN/GaN interface was also detected by capacitance-voltage measurements. However, the field effect was accompanied by a relative large shunt current through the GaN buffer which clearly demonstrates the need for further reduction of the buffer conductivity.

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